



**孕龍科技股份有限公司**  
**Zeroplus Technology Co., Ltd.**

# SPECIFICATION

**MODEL: B12012-IDE**

**PART NO :** \_\_\_\_\_

**VERSION :** V1.00

Approver		Check	Design
GM	PM		

Customer Confirm

\* Please fax the file to  
Zeroplus Technology after  
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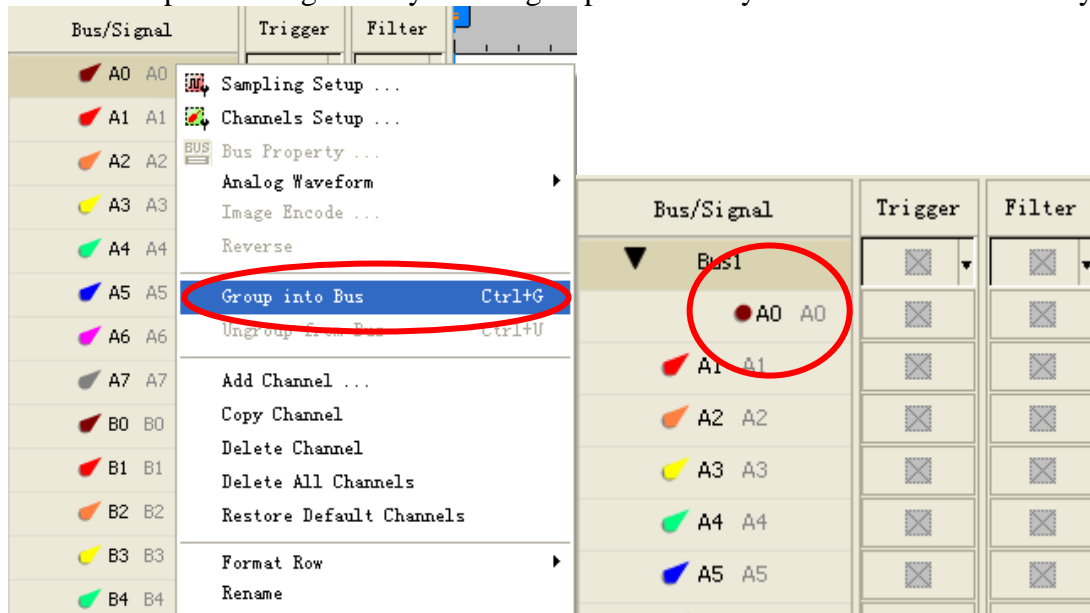
## 1 Software Register

Please register the software as the following steps:

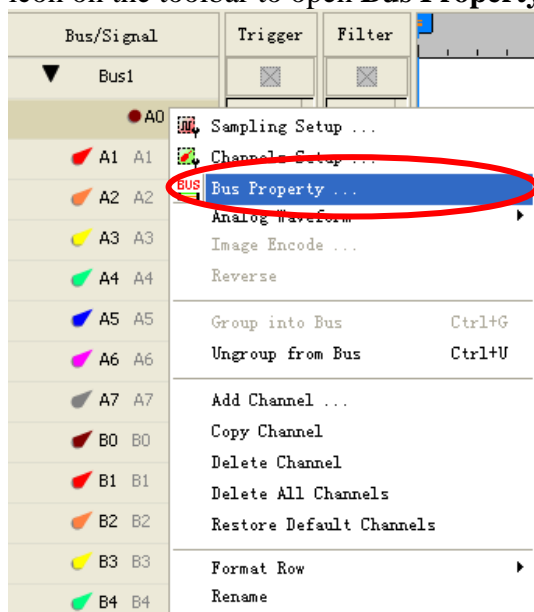
※ Remark1: The registration steps for all protocol analyzers are the same; you can complete the registration by following procedures. Following is an example on how to register the Protocol Analyzer BUS.

※ Remark2: We won't have additional notice for you, when there is any modification of the module specification. If there is some unconformity caused by the module version upgrade, users should take the module software as the standard.

**STEP 1.** Open the Logic Analyzer and group the unanalyzed channels into **Bus1** by pressing the **Right Key**.

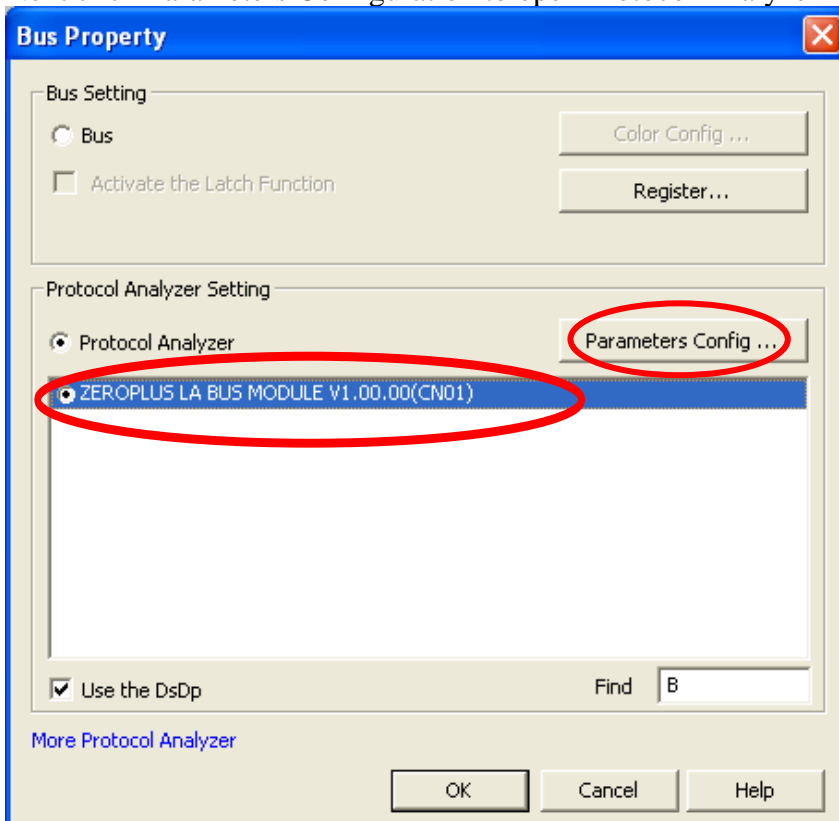


**STEP 2.** Select **Bus 1**, then press **Right Key** on the mouse to list the menu, then press **Bus Property** or **Bus** icon on the toolbar to open **Bus Property** dialog box.

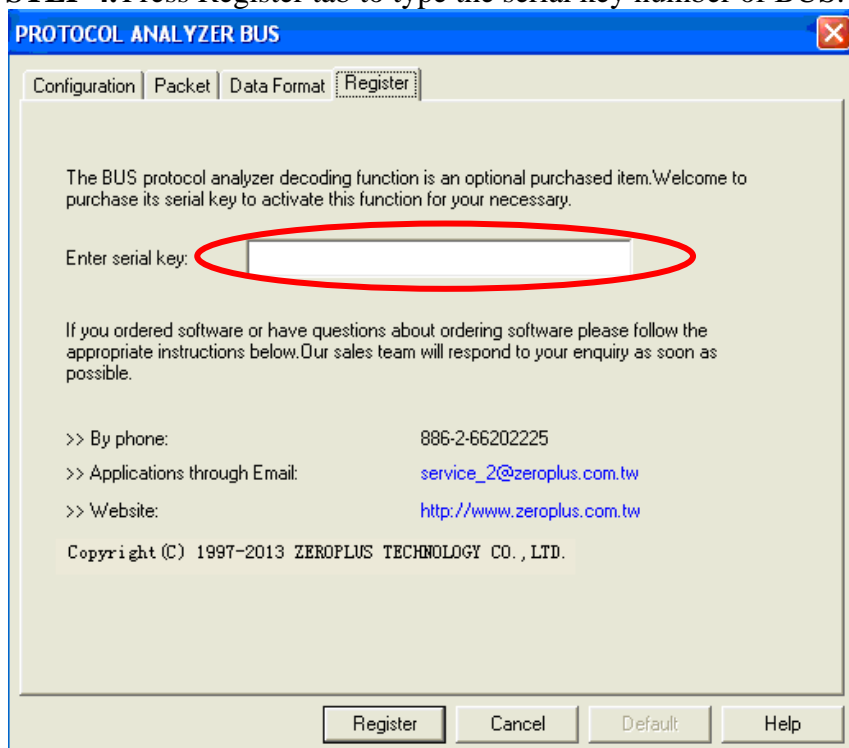




**STEP 3.** Select the Protocol Analyzer, and then choose **ZEROPLUS LA BUS MODULE V1.00.00 (CN01)**. Next click Parameters Configuration to open Protocol Analyzer Bus dialog box.

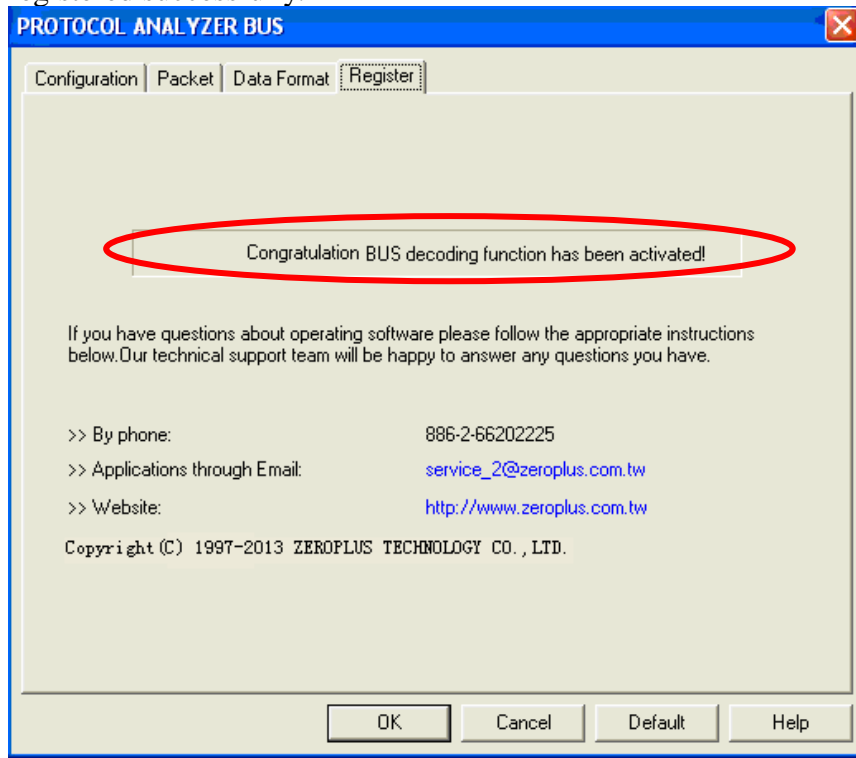


**STEP 4.** Press Register tab to type the serial key number of BUS. Then press Register.





**STEP 5.** After pressing the Register button, following dialog box will appear, it denotes that the BUS has been registered successfully.

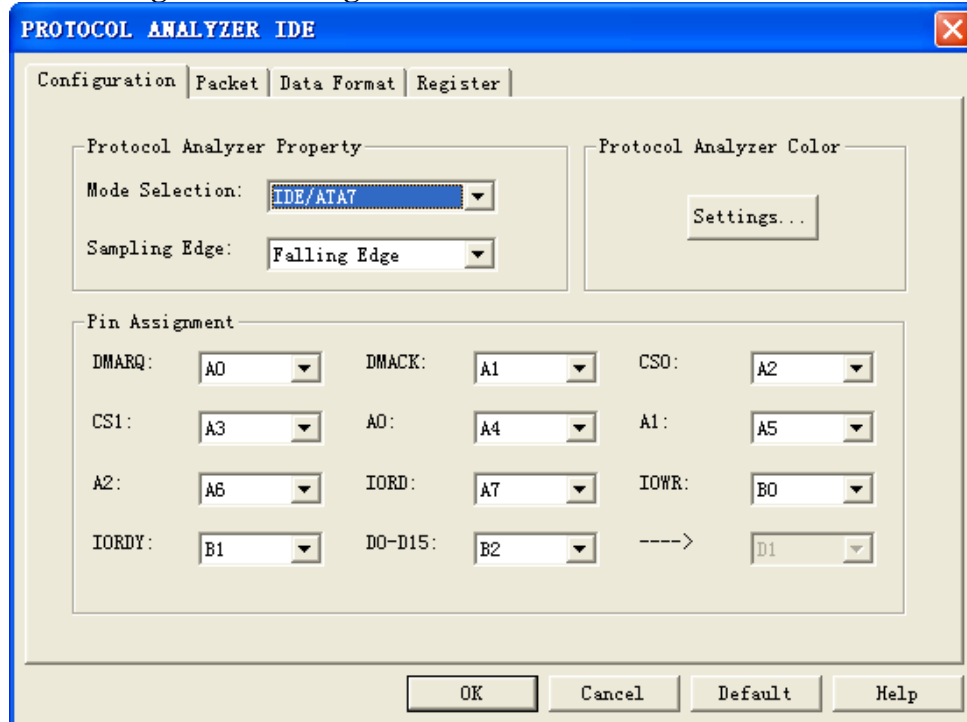




## 2 User Interface

Please refer to the below images to do settings of IDE module.

### IDE Configuration dialog box



#### Mode Selection:

There are now only two work modes: IDE and ATA7 to be selected, some other modes are possible to be added in the future.

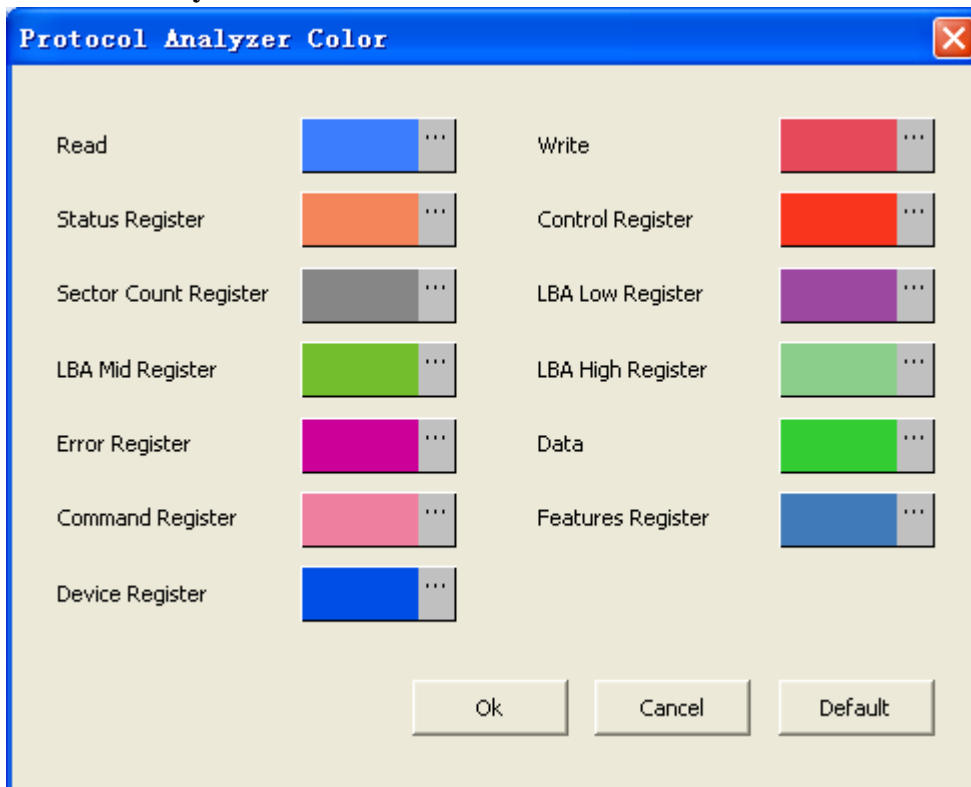
**Sampling Edge:** Rising Edge and Falling Edge can be selected. It is Falling Edge by default.

#### Pin Assignment:

IDE needs twenty-six channels to decode signal at least. DMARQ is used to activate the DMA Mode; DMACK is used to response DMA; CS0 and CS1 are the selecting data; A0, A1 and A2 are the address of register; IORD is used to read data; IOWR is used to write data; IORDY is used to suspend data, and D0~D15 are the data lines.

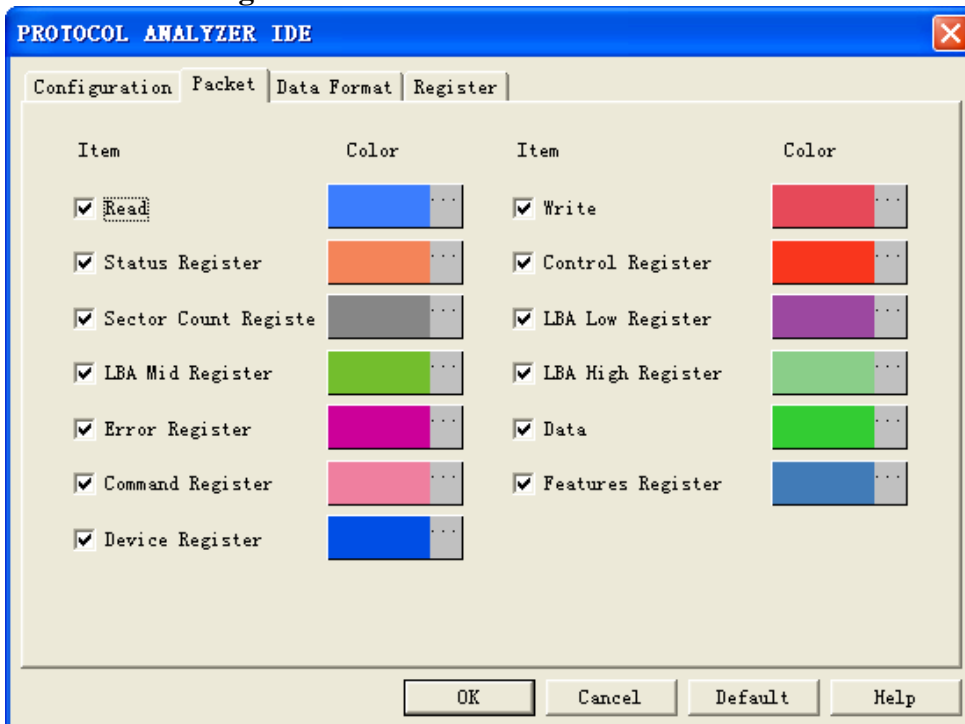


## Protocol Analyzer Color:



The color can be varied by users.

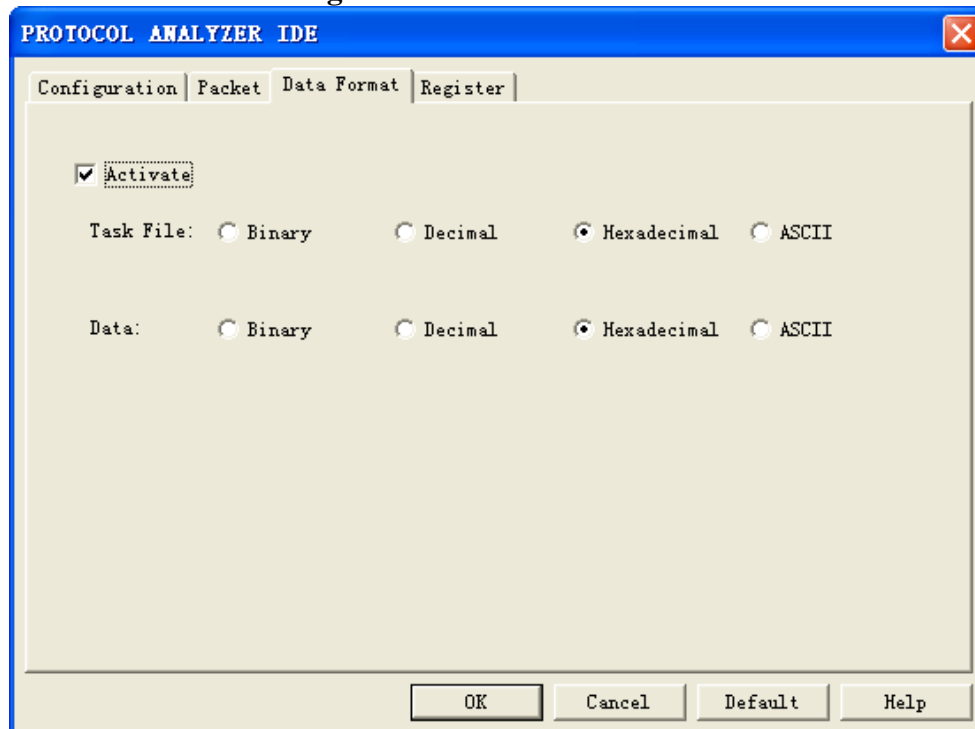
## IDE Packet dialog box



In the Packet part, users can select the items to be displayed and the colors as their requirements.



### IDE Data Format dialog box



Users can set the Data Format as their requirements. The two items (Task File and Data) can be set as Binary, Decimal, Hexadecimal or ASCII (Hexadecimal by default). When selecting the option “Activate”, the format is decided by the settings in the Protocol Analyzer; when not selecting the option “Activate”, the data format is decided by the settings in the main program.

### IDE Register dialog box



There is Zeroplus company information. If you have questions about software operations, you can contact Zeroplus by Telephone or Email.





### 3 Operating Instructions

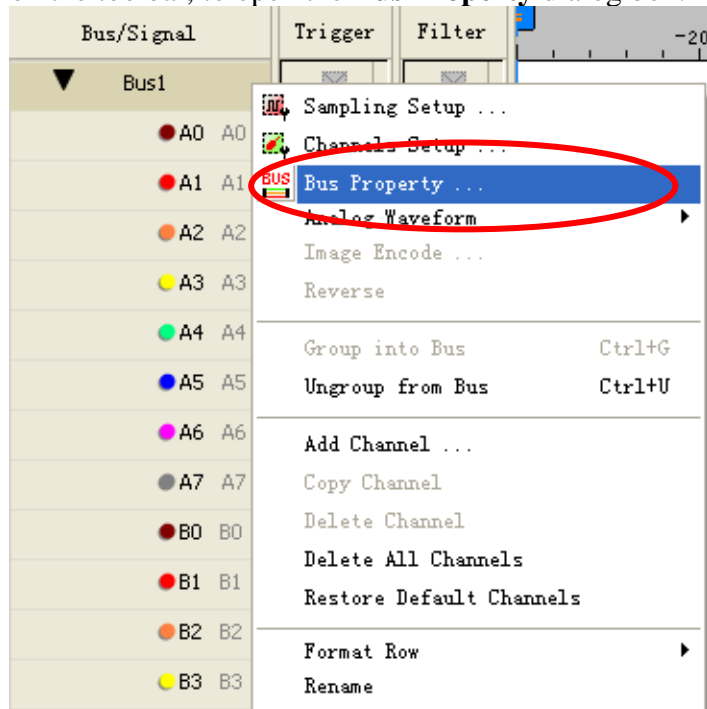
**STEP 1.** Group A0-D1 into **Bus1** by pressing the **Right Key** on the mouse. IDE needs twenty-six channels to decode signal at least, so it is necessary to group twenty-six or more channels into the Bus.

The screenshot shows the software interface with a context menu open over the channel list. The menu options are: Sampling Setup ..., Channels Setup ..., Bus Property ..., Analog Waveform, Image Encode ..., Reverse, **Group into Bus Ctrl+G**, Ungroup from Bus Ctrl+U, Add Channel ..., Copy Channel, Delete Channel, Delete All Channels, Restore Default Channels, Format Row, and Rename. The 'Group into Bus Ctrl+G' option is highlighted with a red oval. The channel list on the left includes A0-A7, B0-B7, C0-C7, and D0-D7. The table on the right has columns for Bus/Signal, Trigger, and Filter. A red oval highlights the 'Bus1' entry in the Bus/Signal column of the table.

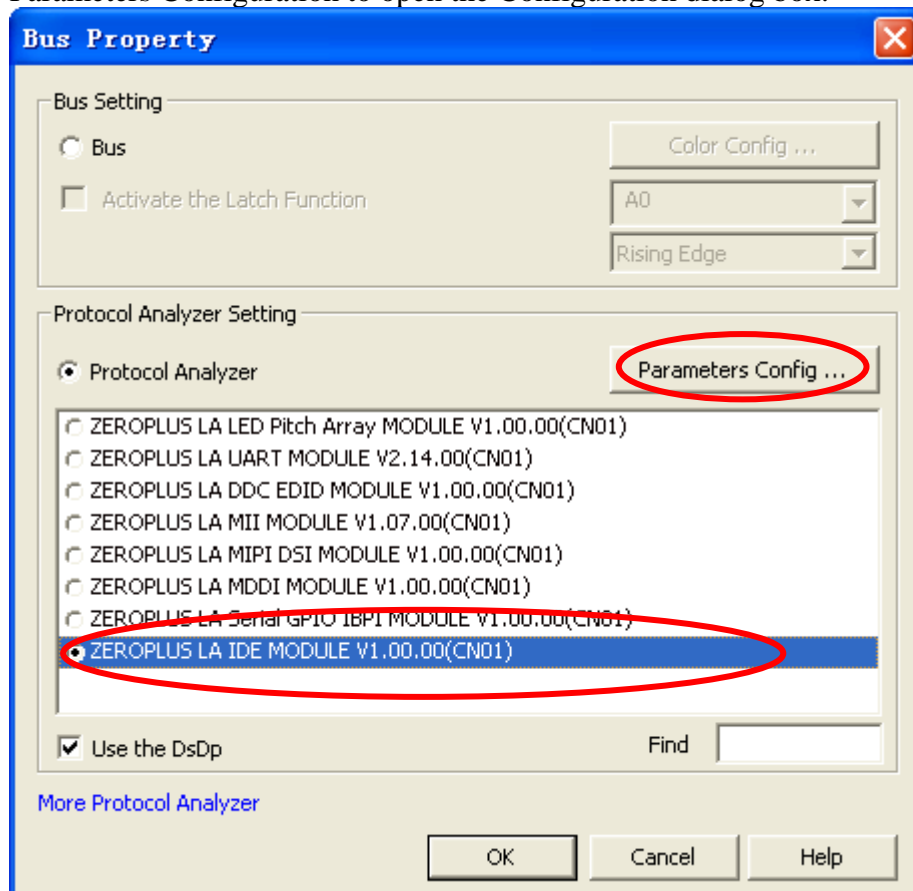
Bus/Signal	Trigger	Filter
Bus1		
A0 A0		
A1 A1		
A2 A2		
A3 A3		
A4 A4		
A5 A5		
A6 A6		
A7 A7		
B0 B0		
B1 B1		
B2 B2		
B3 B3		
B4 B4		
B5 B5		
B6 B6		
B7 B7		
C0 C0		
C1 C1		
C2 C2		
C3 C3		
C4 C4		
C5 C5		
C6 C6		
C7 C7		
D0 D0		
D1 D1		



**STEP 2.** Select **Bus1**, press right key and select **Bus Property** from the popped menu, or click the **Bus** icon on the toolbar, to open the **Bus Property** dialog box.



**STEP 3.** Select Protocol Analyzer, and select ZEROPLUS LA IDE MODULE V1.00.00 (CN01). Then click Parameters Configuration to open the Configuration dialog box.





#### STEP 4. Set the Mode Selection.

**PROTOCOL ANALYZER IDE**

Configuration | Packet | Data Format | Register

Protocol Analyzer Property

Mode Selection: **IDE/ATA7**

Sampling Edge: **Falling Edge**

Protocol Analyzer Color

Settings...

Pin Assignment

DMARQ:	A0	DMACK:	A1	CS0:	A2
CS1:	A3	AO:	A4	A1:	A5
A2:	A6	IORD:	A7	IOWR:	B0
IORDY:	B1	DO-D15:	B2	----	D1

OK Cancel Default Help

#### STEP 5. Set the Sampling Edge.

**PROTOCOL ANALYZER IDE**

Configuration | Packet | Data Format | Register

Protocol Analyzer Property

Mode Selection: **IDE/ATA7**

**Sampling Edge: **Falling Edge****

Protocol Analyzer Color

Settings...

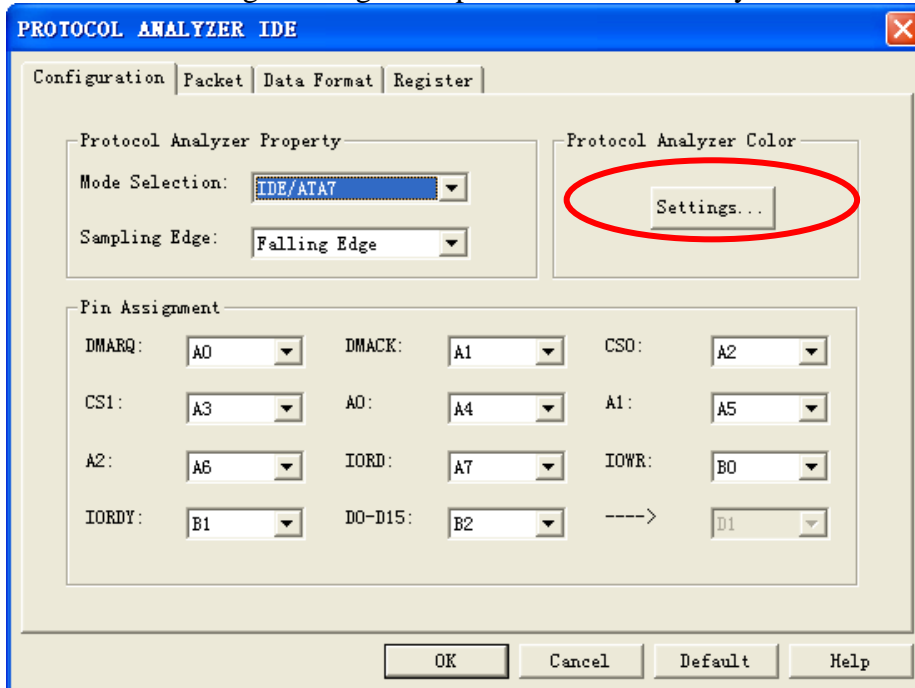
Pin Assignment

DMARQ:	A0	DMACK:	A1	CS0:	A2
CS1:	A3	AO:	A4	A1:	A5
A2:	A6	IORD:	A7	IOWR:	B0
IORDY:	B1	DO-D15:	B2	----	D1

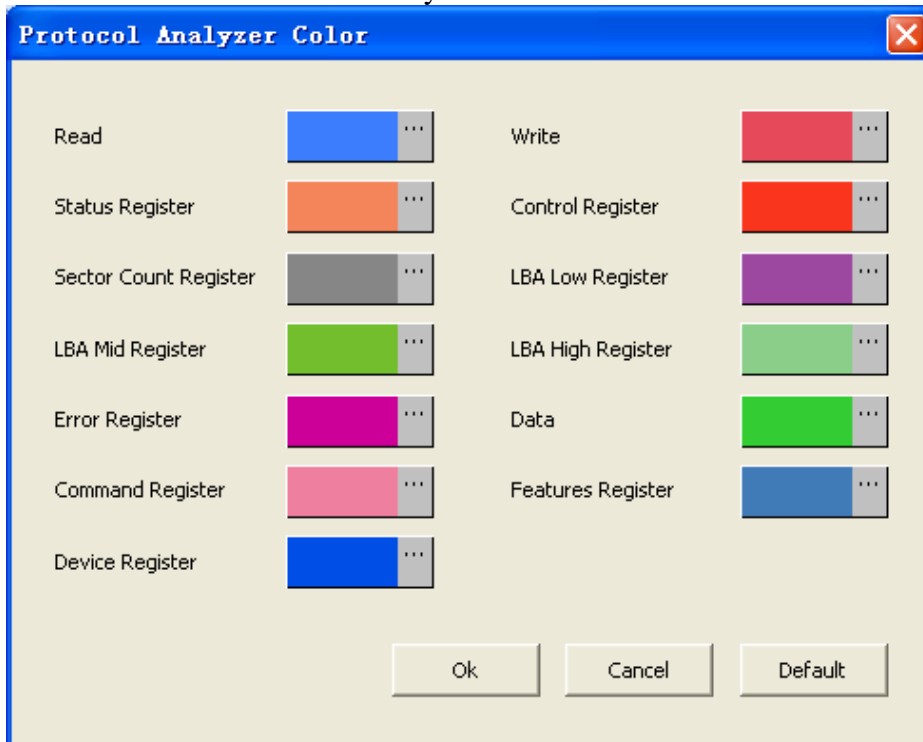
OK Cancel Default Help



**STEP 6.** Pressing “Settings” to open the Protocol Analyzer Color dialog box.



**STEP 7.** Set the Protocol Analyzer Color.





**STEP 8.** Set the Pin Assignment.

**PROTOCOL ANALYZER IDE**

Configuration | Packet | Data Format | Register

Protocol Analyzer Property

Mode Selection: IDE/ATA7

Sampling Edge: Falling Edge

Protocol Analyzer Color

Settings...

**Pin Assignment**

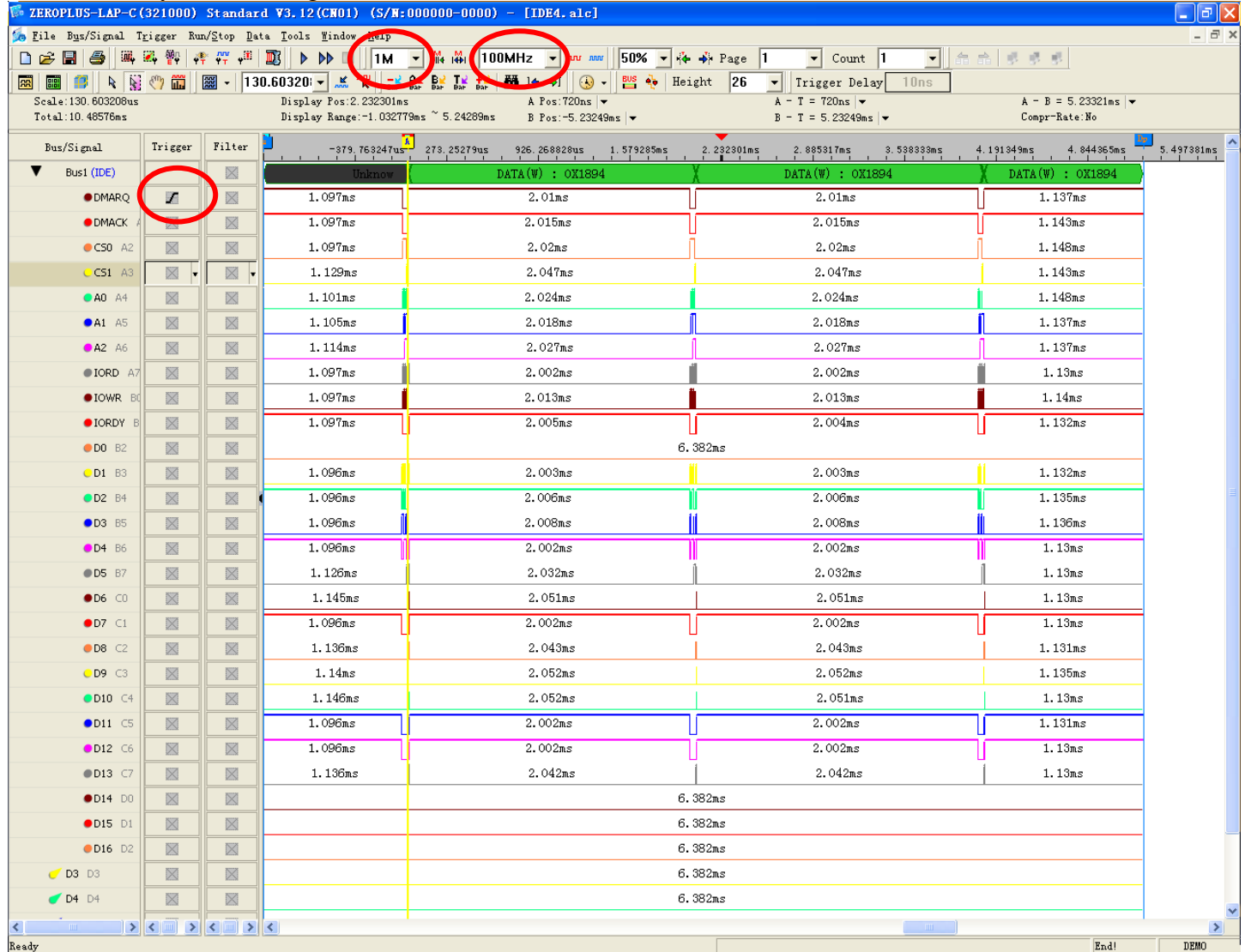
DMARQ:	A0	DMACK:	A1	CS0:	A2
CS1:	A3	AO:	A4	A1:	A5
A2:	A6	IORD:	A7	IOWR:	B0
IORDY:	B1	D0-D15:	B2	----	D1

OK Cancel Default Help



**STEP 9.** Following pictures show the completion of the protocol analyzer decoding and the packet list. The trigger condition is set as Rising Edge, the memory depth is 1M and the sampling frequency is 100MHz (the sampling frequency should be more than four times higher than the signal to be tested).

### Protocol Analyzer Decoding





## Packet List

